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Zitiervorschlag im APA Stil:

Bhattacharyya, M., Dusch, B., Jansen, D., & Mackensen, E. (2015). Design and Verification of a Mixed-Signal SoC for Biomedical Applications. *Tagungsband zum Workshop der Multiprojekt-Chip-Gruppe Baden-Württemberg*, *54*, 43–48. https://nbn-resolving.org/urn:nbn:de:bsz:ofb1-opus4-60382

Abstract

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***Abstract*—In this paper an RFID/NFC (ISO 15693 standard) based inductively powered passive SoC (system on chip) for biomedical applications is presented. A brief overview of the system design, layout techniques and verification method is discussed here. The SoC includes an integrated 32 bit microcontroller, sensor interface circuit, analog to digital converter, integrated RAM, ROM and some other peripherals required for the complete passive operation. The entire chip is realized in CMOS 0.18 µm technology with a chip area of 1.52mm x 3.24 mm.**

***Keywords*—RFID (Radio Frequency Identification Device), RF–field passive system, energy harvesting, analog to digital converter, sensor interface circuitry, microcontroller, biotelemtry.**

I. Introduction

Near field communication (NFC) along with RFID technology has gained significant importance in recent times which in turn aids in development of passive sensor systems by harvesting energy from the induced electromagnetic field [1]. NFC provides a new opportunity for the development of ultra-low power sensor systems for biotelemetry applications. This is because a commercially available hand held device like a smart phone or a tablet is good enough to interact with such a system.

For this reason a SoC with NFC interface, sensor interface circuitry, SAR ADC, microcontroller core and memory have been developed. Although the end application of this SoC is not fixed, the one intended application is to develop a completely passive biotelemetry system to monitor blood pressure in arterial system (femoral) for the patients suffering from Peripheral Arterial Disease (PAD) [2], much similar to the work presented in [3]. Due to availability of features like programmable instrumentation amplifier, integrated temperature sensor and availability of virtual ground compatible with human body model it can also be used for measuring ECG signal, body temperature [4] etc.

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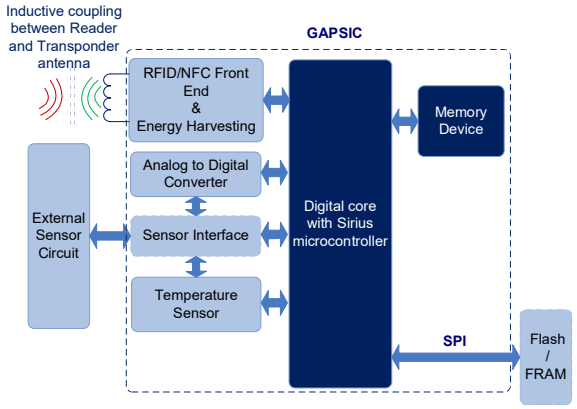

Figure 1: System overview for the proposed SoC (GAPSIC).

A system overview will be presented in section II. Section III and IV contain the description for the analog and the digital part and some basic layout techniques are described in brief in section V.

II. System Overview

The basic system overview of the developed SoC – GAPSIC (*General Application Passive Sensor Integrated Circuit*) is shown in the figure 1 with all the necessary important blocks. The antenna serves the dual purpose which is used for RFID/NFC communication as well as for harvesting energy by using inductive coupling. The sensors can be externally connected to the system depending on the intended area of applications. The Flash/FRAM contains the application software or the firmware which can be updated depending on the requirement for the application. The internal digital core can communicate with the external device by using SPI interface. The analog to digital converter is a charge redistribution type based on Successive Approximation Register logic (SAR). The sensor interface includes the programmable instrumentation amplifier along with a channel selector and a virtual ground amplifier. The internal bandgap reference is modified to act as a temperature sensor whose purpose is to measure the internal temperature of the chip which is helpful in doing temperature dependent calibrations. The digital core consists of the core of

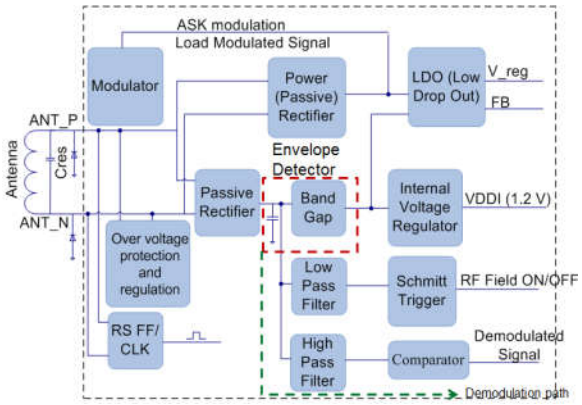

Figure 2: Simplified block diagram of the RFID/NFC analog frontend.

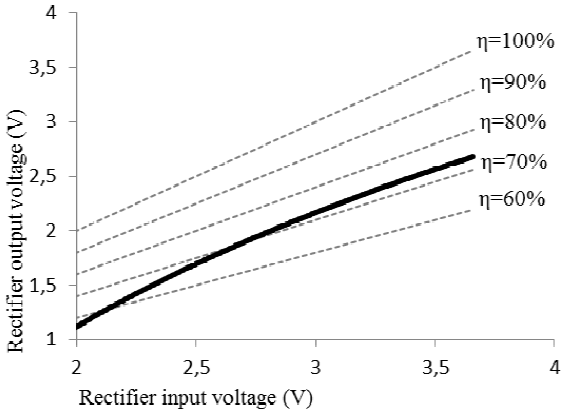

Figure 3: Measured efficiency of the energy harvesting rectifier (shown in solid line).

the SIRIUS microcontroller along with other peripherals like timer, interrupt controller etc. The internal memory devices include a 16 kB ROM and a 16 kB RAM. Being a mixed signal IC it consists of an analog part and a digital part, so each of the system blocks is described further accordingly.

III. Analog Part

The analog part consists of an RFID/NFC block along with an energy harvesting part and the sensor interface part including the analog to digital converter.

A. RFID/NFC and Energy Harvesting Block

This block consists of the analog circuitry required for RFID/NFC communication and for energy harvesting as shown in the figure 2 [5]. The energy harvesting block consists of a full wave bridge rectifier and a low drop out voltage regulator which provides a stable output voltage. As shown in the figure 3, the rectifier has an average efficiency η of ~ 66 % which provides sufficient energy required for complete passive operation. The low drop out regulator (LDO) uses the harvested energy available from the rectifier to provide a

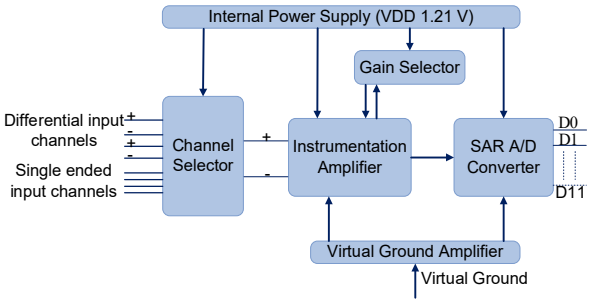

Figure 4: Simplified block diagram of the Sensor interface circuit along with SAR ADC analog frontend.

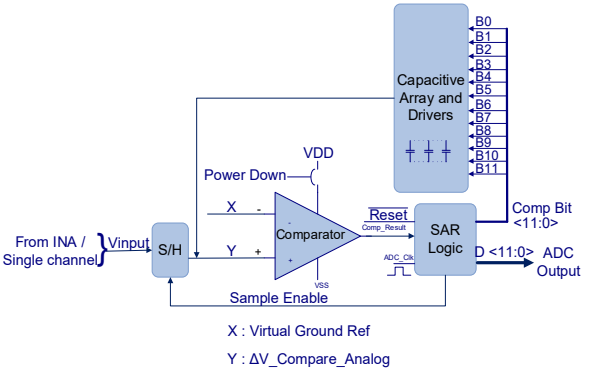

Figure 5: Block diagram showing the sample and hold circuit, comparator, capacitive array and the SAR logic for the Analog to Digital converter (ADC).

stable output voltage ranging from 1.21 V to 2.0 V. The internal bandgap reference voltage provides a stable reference voltage 1.21 V ± 20 mV. The bandgap circuit also act as a load required for the envelope detector circuit (shown in figure 2) which is required for demodulation. Further this bandgap circuit is modified as a temperature sensor in order to get an idea of the in chip temperature, which can be useful for calibration purposes.

The clock is extracted from the RFID field by a clock regenerator circuit which is then further used as system clock. The demodulation is carried out by a comparator which has a predefined offset voltage which sets the dc working condition required for proper demodulation of the RFID signal. The reply is sent back via the modulator circuit which uses ASK (Amplitude Shift Keying) modulation for this purpose.

B. Sensor Interface Circuit and SAR ADC

As shown in figure 4 the sensor interface circuit consists of a channel selector to which two differential channels and four single ended channels are available to which different kinds of sensors can be connected depending on the requirements. The internal low dropout voltage regulator supplies the entire sensor interface block with a constant voltage supply of 1.21 V which in turn aids in lowering the power consumption. In this design, the instrumentation amplifier used is a three operational amplifier instrumentation ampli-

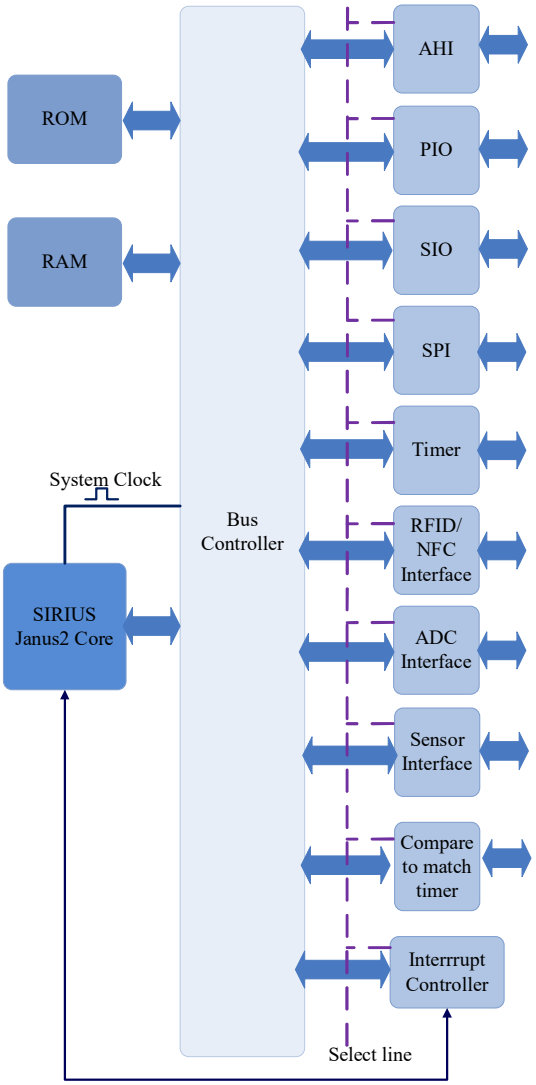

Figure 6: Block diagram showing the digital core including the microcontroller, integrated memory (RAM and ROM) and other peripheries.

fier with a programmable gain. It has a maximum offset voltage of ~2 mV depending upon the temperature range (-30 °C to 85 °C). The gain selector can be controlled by software in order to choose the required gain ranging from 1 to 100. Due to availability of a digital part and microcontroller no offset cancellation method is used rather the offset is measured before every measurement and the value is stored for cancellation. The virtual ground amplifier is designed in such a way that it is compatible with the human body model so that one can use it as the reference electrode in case of an ECG measurement [6].

As shown in the figure 5 the SAR ADC block consists of a sample and hold circuit, comparator, capacitive array with drivers and SAR logic [7]. The sample and hold circuit switch is designed in such a way that it has minimum ohmic resistance as well as the charge injection is also low. The comparator is an open loop comparator with high input impedance but very low input capacitance as it will affect the measurement results. The input offset voltage of the comparator is kept as low as possible (60 µV to 150 µV depending on the temperature). The effect of the random mismatch is reduced effectively by adopting effective layout techniques. The maximum input frequency is around 20 kHz which is well within the specified range of operation. The capacitive array consists of unit capacitances arranged in binary form representing each bits from 1 to 12. In order to avoid the effect of line impedances each of the unit capacitances has their own driver stage. The SAR logic consists of a binary logic required for the measurement in successive approximation form which is actually provided in the digital block. In general, except the voltage regulator, the entire sensor interface circuitry block can be isolated or kept switched off when not in use thereby reducing the static power consumption as much as possible. The layout of the capacitive array is very important and successful layout is necessary for proper operation which is discussed later.

IV. Digital Part

The digital part includes the SIRIUS JANUS 2.0 microcontroller, memory devices (RAM and ROM) and other peripheries as shown in the figure 6. Some of the individual blocks are discussed below [8]. The select line shown in the figure helps to select each of the peripheries as and when required. The other signal lines which are not shown in the figure for the sake of simplification are read, write, reset, address bus and system clock. Each of the peripheries is selected by using their corresponding addresses and the select lines.

A. SIRIUS JANUS 2 Core

The microcontroller used here is SIRIUS JANUS 2.0 which is developed by ASIC design center (University of Applied Sciences, Offenburg), based upon Von Neumann architecture. It has 16 bit data bus and 32 bit address bus. It consists of 16 registers of which 12 are universal and 4 are special registers. The arithmetic and logical operations are based on Reduced Instruction Set Computing (RISC). The internal control unit can handle 16 bit command format along with an internal 8 bit control signal.

The microcontroller is designed to operate at much higher frequency (~ 50 MHz), but here it is operated at a frequency of 6.78 MHz. The extracted RFID clock is divided to half and then further used as the system clock. The intended application doesn't require a higher clock frequency hence no external oscillator or an internal PLL (Phase locked loop) is required which helps to keep the overall size smaller and also reduces the power consumption which is important for passive operation. Also a slower system clock means lower

power consumption which is again important for power consumption.

B. Audio Human Interface (AHI)

This is not required for the actual operation of the chip but only used for easy debugging purposes. Different frequencies can be set at different point of operation which is useful to identify the current state of the system. This is more of a use in the development phase rather than the actual application.

C. Parallel Input Output (PIO)

Similar to the AHI block the PIO block is also used for debugging by using the 8 bit data bus to read or to write.

D. Serial Input Output (SIO)

Like the AHI block and PIO block this is also used for debugging purposes as text messages used for detecting errors can be read over Hyper Terminal. This is a very useful debugging tool which can be extensively used in the development phase.

E. Serial Parallel Interface (SPI)

This is used mainly for the external memory device which can be a Flash or FRAM, to load the firmware from the external memory into the internal RAM. It uses the standard SPI signals MISO (Master input slave output), MOSI (Master output and slave input), SPI clock and chip selects (two are available). The first chip select is by default set for the selection of the external memory device and one more chip select is free to be used for some other SPI device.

F. Timer

There are in total four timers available out of which one is used for boot up routine and the other one is used by the RFID communication. The other two timers are completely free and can be used at any given time.

G. RFID/NFC Interface

This block is very important as it is responsible for the digital logic required for the RFID and NFC communication as well as the generation of the system clock. It generates four interrupt signals required for the RFID/NFC communication.

H. ADC Interface

The ADC interface consists of the SAR logic, ADC clock prescaler, data registers and control registers. The SAR logic block contains the binary logic required for the ADC operation. The clock prescaler is useful as one can chose the clock frequency required for the ADC operation (~96 kHz to ~1 kHz). When

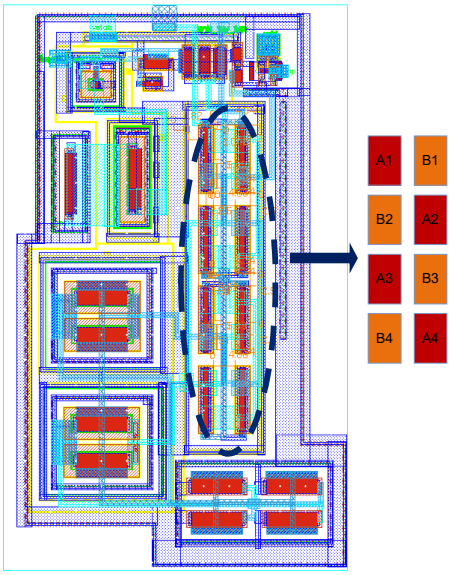

Figure 7: SAR ADC comparator layout showing the common centroid layout for the differential pair which is divided into two sub pairs each.

the ADC conversion is finished it generates an interrupt. The ADC conversion result is stored in a data register which can be read as and when required till the next conversion starts or a reset occurs.

I. Sensor Interface

The sensor interface consists mainly of control and data registers required to control the sensor interface port of the analog part except the ADC. It controls the power on and off for the entire sensor interface part, selection of the channel required for measurement and also the gain of the instrumentation amplifier.

J. Compare to Match

The compare to match is used as a pulse generator which can be useful for some measurement purposes for example in case of impedance measurement. A pulse wave is useful as it reduces the galvanic corrosion in electrodes due to the DC (Direct Current) effect.

K. Interrupt controller

The interrupt controller consists of several registers which can be controlled via software such as control, edge, mask and base address registers. The control register has two bits, one of them being responsible to choose the mode (16 or 32 bit) and the other one is used to reset any pending interrupt. For this design the 16 bit mode is chosen. In the edge register one can decide between rising edge and falling edge to trigger the respective interrupt. The mask register decides which interrupt source will trigger the interrupt and

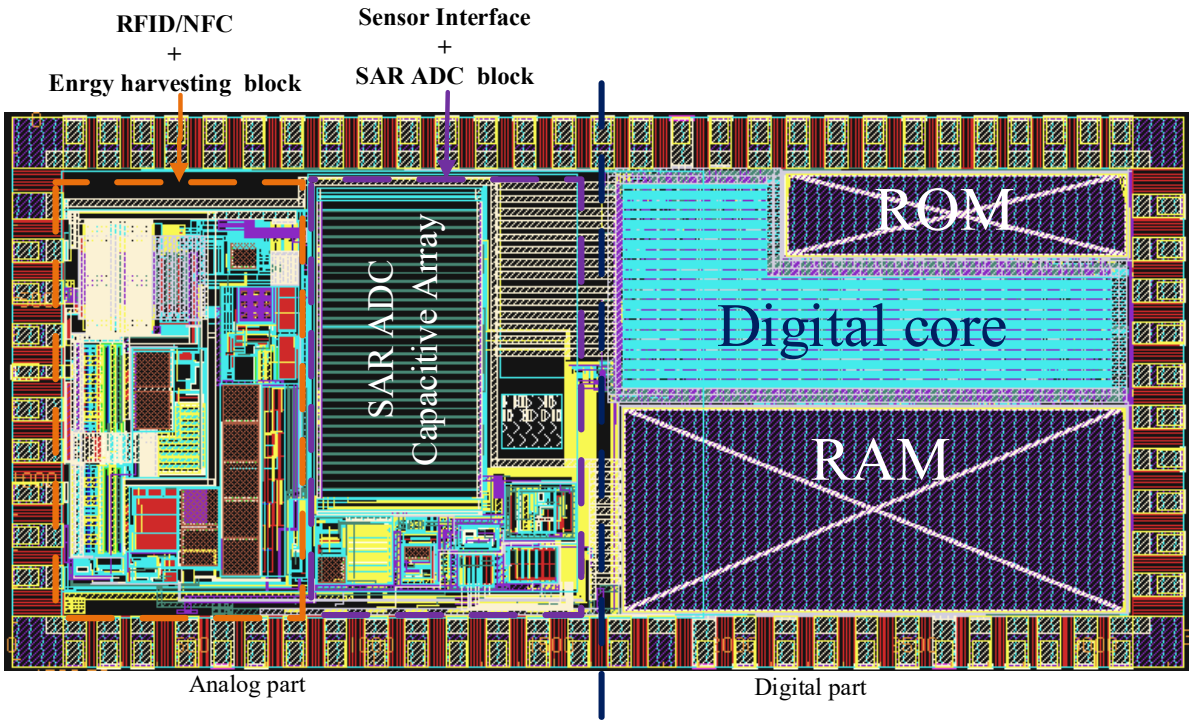

Figure 8: Complete layout of the SoC along with the bond pads.

the bit 0 is non maskable as it is only readable. The base address register contains the base address for the hardware interrupts which is further organized in a vector table.

L. Random Access memory (RAM)

A 16 kB RAM is provided inside the chip, the entire firmware along with the initial routines is organized inside the RAM.

M. Read only memory (ROM)

The ROM is also 16 kB which contains the initial boot up routine which is mainly the SPI routine along with the hardware initialization required for the operation. The SPI routine in the ROM interacts with the SPI block and starts the SPI communication required for SPI read operation which uploads the firmware from the external memory device into the RAM. Moreover it also contains a small program which responds every time there is a RFID/NFC inventory command by sending a unique identification number. This is also a part of the initial boot up check for the system.

V. Layout Techniques

As it is a mixed signal system the digital layout is accomplished by using Cadence Encounter program and the analog part is done in Cadence Virtuoso. Finally both parts are combined together in Cadence Virtuoso program along with the bond pads. Here some of the layout techniques adopted for the analog part are discussed in brief.

In general for critical circuits like the comparator (as shown in figure 7) for ADC or instrumentation amplifier, special care has been taken while doing the layout. The layouts of the differential pairs are done by using a common centroid approach in order to reduce the error due to random offsets occurring due to random mismatches. Also guard rings are provided around the transistors for better noise immunity. In figure 7 A1, A2, A3 and A4 represent one of the differential pair and B1, B2, B3 and B4 represent another differential pair which are then arranged in zig – zag form in order to reduce the effect due to random mismatches.

A partial common centroid layout approach is adopted for the layout of the capacitive array in order to reduce the effect due to gradients caused by temperature as well as oxide thickness [9]. For the digital circuit layout, the clock trees are designed for much higher frequencies than required to operate, so that the delays are minimal. Figure 8 shows the complete layout of the chip where on the left hand side is the analog part and the right hand side is the digital part along with the memory devices (RAM and ROM).

VI. Design Simulation and Evaluation

The analog part is verified by using different kinds of simulations (e.g. corner and Monte Carlo simulations) as well as post layout extraction which is important to take into account all the parasitics which

Table 1: Overall features of the frontend.

Technology	UMC CMOS 0.18 µm
Size of the chip	1.52 mm × 3.24 mm
Bandgap reference voltage	1.21 V ± 20 mV
Temperature range	-30 °C – 85 °C
Output range of Low drop out regulator	1.21 V – 2.2 V
System clock	6.78 MHz
RFID / NFC standard	ISO 15693
ADC	SAR , 12 bit resolution (max)
ADC channel	Two differential and four single ended
Sensor Interface power consumption (max)	~ 570 µW
Mode of operations	Passive or semi-passive
Application area	Biotelemetry, industrial sensors

play a dominant role in the sensor interface circuit and ADC. A mixed-signal simulation has been used for the simulation of the SAR ADC in order to verify the complete functionality. For the digital part other than simulation one can realize the entire design in an FPGA (Field Programmable Gate Array). For this purpose a FPGA emulation board is used along with an analog circuitry interface consisting of RFID/NFC in order to realize the complete system. A post layout simulation is also done with the generated netlist from encounter. The external memory devices are also included while doing the simulation in order to realize the exact one to one system performance.

VII. Conclusions

An ultra-low power consuming SoC for biotelemetry applications has been discussed and a brief overview of the overall features of the SoC is presented in table 1. The SoC consists of an RFID/NFC frontend which is used for communication as well as for energy harvesting which is important for passive operation. A 12 bit SAR ADC sensor interface circuit along with a 32 bit microcontroller opens up a wide range of applications. Although the intended area of application is in the field of biotelemetry it can also be used for passive industrial sensors [10]. The availability of the RFID/NFC communication standard (ISO 15693) makes it easy to interact with such a system as a standard hand held device like a smart phone or a tablet containing application software can be used by the end user to interact. This opens up new opportunities for next generation passive medical health care systems [11].

Acknowledgement

The authors like to thank all colleagues from ASIC design center and Institute for Applied Research Offenburg for their support and coordination.

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