Compact Modeling of Inkjet Printed, High Mobility, Electrolyte-Gated Transistors

Gabriel C. Marques, Suresh K. Garlapati, Simone Dehm, Subho Dasgupta, Jasmin Aghassi and Mehdi B. Tahoori

Abstract—High mobility, electrolyte-gated transistors (EGTs) show high DC performance at low voltages (< 2 V). To model those EGTs, we have used different models for the below and the above threshold regime with appropriate interpolation to ensure continuity and smoothness over all regimes. This empirical model matches very well with our measured results obtained by the electrical characterization of EGTs.

Index Terms—Electrolyte-gated field-effect transistors, Semiconductor Oxide based devices, Printed electronics

I. Introduction

The field of Printed Electronics (PE) is a promising, young research area where the devices or electronic circuits are typically printed on flexible substrates. The flexible substrates lead to interesting applications, for instance in photovoltaics [1], radio frequency identification (RFID) tags [2], smart sensors [3], wearables [4], etc. In future, printed devices, like transistors, can play a key role within the *Internet of Things*, where computers and sensors are linked together into personal, everyday items [5]. In PE, usually field-effect transistors based on organic materials (OFETs) are used for the circuit design. However, OFETs exhibit low field-effect mobility values and a short lifetime under ambient conditions [6], [7], which finally results in low performable and lifetime-limited circuits.

Electrolyte-gated field-effect transistors (EGTs) based on inorganic semiconductor oxides present themselves as an alternative to the above mentioned OFETs, especially in the low voltage regime. The low temperature required for the process [8], enables the usage of flexible plastic foils as substrates. Furthermore, EGTs with oxide semiconductors exhibit higher field-effect mobility values as well as thermal and long term stabilities even at lower voltage ranges [8] - [11].

A model, which might be used in the design of circuits based on EGTs, must capture the device characteristics accurately. A further requirement is that the modeled slopes must be continuous and smooth over all regimes in order to be integrated into circuit simulators, e.g. SPICE. For this purpose, several groups [12] - [15] have used a universal model [16] for amorphous thin film transistors (a-Si:H TFTs). However, the universal model does not reproduce the behavior of our EGTs and only considers voltage ranges above the threshold voltage V_{TH}. The high number of input parameters, that are necessary for the universal model, are also disadvantageous.

In this context, we use different models for the below and the above threshold regime [17]. The below threshold regime is modeled with the subthreshold swing model [16] and for the linear as well as the saturation regimes, an altered form of the Curtice model, originally developed for gallium arsenide field-effect transistors (GaAs FETs) [17] is employed. Regarding device and circuit simulations, continuity and smoothness are important criterions of a model. To ensure continuity and smoothness over all the regimes, an interpolation scheme is applied between the sub- and superthreshold regions. Before interpolating, the respective input parameters must be extracted from experimental data (output and transfer curves). The parameter extraction is done on a device with a W (channel Width) / L (channel length)-ratio of 1. For other W/L-ratios, the output current must just be multiplied with the W/L-ratio of interest. In case of input parameters change by replacing the materials for instance, the extraction routine must be repeated from beginning. Applying the methodology to our EGTs, the results show very reasonable agreements between measured and modeled curves.

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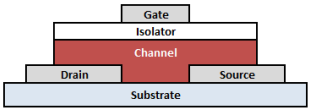

Figure 1: Cross-section view of an organic field-effect transistor

The organization of this paper is as follows. In Section 2, the technology used for our EGTs and the device characteristics are presented. Section 3 describes the modeling methodology. In Section 4 the accuracy of the model is shown on a modeling example. Finally, Section 5 concludes the paper.

II. Technology

Organic p-type transistors are frequent but n-type organic transistors are still rare in Printed Electronics. A popular architecture of an OFET is known as the top-gate bottom-contact configuration (Figure 1). In the top-gate bottom-contact configuration an organic material, e.g. poly(3-hexylthiophen-2.5diyl)(P3HT), acts as channel between two metal electrodes (source and drain). On top of the channel follows an organic or inorganic insulator, which is sandwiched between the channel and a further metal electrode (gate). While the field-effect mobility is improved from $< 10^{-3}$ $cm^2(Vs)^{-1}$ to 1 $cm^2(Vs)^{-1}$, since the first reported OFET in 1989, the typical supply voltages are still quite high (>> 20 V) .

To overcome the low field-effect mobility and the high voltage, which is a requirement for OFETs to perform well, an electrolyte-gated transistor based on an inorganic semiconductor oxide was proposed in [11]. Instead of a p-conducting channel, the EGT has an n-conducting channel, which is based on indium oxide (In_2O_3). Comparing EGTs with OFETs, the field-effect mobility of the semiconductor oxide based EGT (126 $cm^2(Vs)^{-1}$ in [11]) exceeds those of OFETs by orders of magnitude. The voltage range required for the EGTs ($\leq$ 2 V) is also smaller than the voltage range of a typical OFET, which makes it suitable for low-voltage applications.

Therefore, the transistor channel is based on an inorganic semiconductor and a solid polymer electrolyte forms the gate dielectric. The electrolyte-gating allows operating the devices at lower voltage ranges. By applying a positive potential on the gate, anions from the electrolyte are attracted to the gate-electrolyte interface. At the same time, cations migrate to the electrolyte-semiconductor interface, which causes accumulation of electrons inside the channel at the electrolyte-semiconductor interface. The accumulation of charges and ions at each interface leads to two electrical double layers (EDLs), known as the Helmholtz double layer (Figure 2) [20]. The formation of a

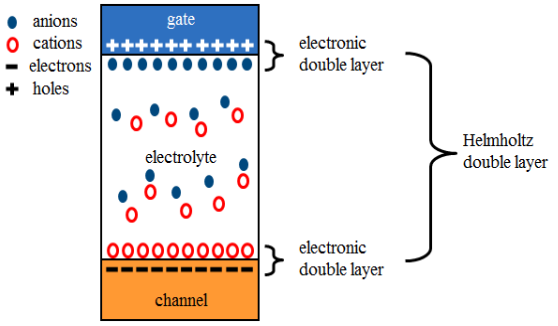

Figure 2: Formation of a Helmholtz double layer by applying a positive voltage to the gate

Helmholtz double layer results in a high gate capacitance (4.33 µF/cm^2 in [11]). The high gate capacitance in combination with high mobility channel materials results in high DC-performable devices [10], [11], [20]-[22].

Besides the high DC performance of EGTs, the device fabrication is very straightforward. First, the passive structures (source, drain and gate) are structured by lithography or laser ablation on a substrate. After structuring the electrodes, the channel is printed between source and drain with an inkjet printer. Then, the electrolyte is printed in a way that the channel and partially the gate electrode are covered by the electrolyte. In the last step (PEDOT:PSS), a conducting polymer, is printed on top of the electrolyte as top-gate.

III. Compact Modeling

For the silicon technology, a broad spectrum of transistor models are available. Some of the models, developed for silicon based transistors, can be adopted to model the printed transistors [12], [14], [23]. Within the overall range of transistor models, a universal model (AIM-SPICE level 15 model [24] or HSpice Level 61 model [25]) for amorphous thin film transistors (a-Si:H TFTs) [16] has gained a lot of attention. The popularity of the model is related to the fact that printed transistors have some similarities with a-Si:H TFTs [14], e.g. both are accumulation based devices. However, the AIM-SPICE level 15 model has a high number of input parameters, which first need to be extracted. In [12], [14], the unified model and parameter extraction method (UMEM) [26] is utilized to extract the parameters for the AIM-SPICE level 15 model, applied on an OFET. When we have employed UMEM to our inorganic oxide based EGTs, an accurate match between the modeled and the measured results is not possible. Therefore our objective has been to model EGTs with an accurate model, which has at the same time the lowest number of possible input parameters. Additionally, to avoid convergence problems in circuit simulation, the model behavior must be continuous and smooth.

Table 1: Summary of extracted input parameters needed for the electrolyte-gated transistor model

Parameters	Below Threshold	Near Threshold	Above Threshold
$Dn\ [cm^2s^{-1}]$	$33.16e^{-3}$	-	-
$I_0\ [A]$	$1.5e^{-10}$	-	-
$n_0\ [cm^3]$	$1.10e^{9}$	-	-
a	-	$213.42e^{-6}$	-
b	-	$-185.88e^{-6}$	-
c	-	$55.32e^{-6}$	-
d	-	$-5.58e^{-6}$	-
$\alpha\ [V^{-1}]$	4	4	4
$\lambda\ [V^{-1}]$	-	-	$50e^{-3}$
$\beta\ [A/V^2]$	-	-	$265e^{-6}$
$V_{TH}\ [V]$	-	-	0.45

To overcome the issues of UMEM, we used a model proposed in [17]. The model is based on the subthreshold swing model [16] for the below threshold regime and a modified version of the Curtice model [17] for the above threshold regime. A cubic interpolation in-between the subthreshold swing and the Curtice model ensure continuity and smoothness over all regimes.

Independent from the *W/L*-ratio of interest, it is recommended to start to model a device with a $W/L = 1$ and afterwards to multiply the output current with the respective *W/L*-ratio.

From [17], the subthreshold regime is modeled with the subthreshold swing model [16]:

$$I_{DS} = \frac{W}{L} q \cdot D_N \cdot n_0 \cdot e^{\frac{V_{GS}}{D_n}} \cdot \tanh(\alpha V_{DS}) + I_0,$$

where W is the channel width, L is the channel length, q is the elementary charge of an electron, D_n is the diffusion coefficient, n_0 is the electron density, α is the fitting parameter describing the knee region, V_{DS} is the drain-source voltage and V_{GS} is the gate-source voltage.

Next, the above threshold regime is modeled with the Curtice model:

$$I_{DS} = \beta(V_{GS} - V_{TH})^2 \cdot \tanh(\alpha V_{DS}) \cdot (1 + \lambda V_{DS}),$$

$$\text{with } \beta = \frac{W}{L} \cdot \mu_{FET} \cdot C_{Gate},$$

where V_{TH} is the threshold voltage, λ is the channel length modulation parameter, μ_{FET} is the field-effect mobility and C_{Gate} is the gate capacitance.

As final step, a cubic interpolation between the below and the above threshold regions ensures continuity and smoothness over all regimes:

$$I_{DS} = (aV_{GS}^3 + bV_{GS}^2 + cV_{GS} + d) \cdot \tanh(\alpha V_{DS}) \cdot (1 + \lambda V_{DS})$$

IV. Results and Validation with Measurements

The experimental data is based on an electrolyte-gated transistor with a printed indium oxide In_2O_3 channel and a *W/L*-ratio of 1. The electrolytic insulator and the PEDOT:PSS (top gate) have also been printed. The EGTs have been electrically characterized with a probe station and a parameter analyzer. In a second step we extracted the model parameters with the proposed methodology in [17] and summarized the results in Table 1. The simulated IV curves and transfer characteristics show a very good agreement with our measurement results (Figure 3). As the model behavior is continuous and smooth, it is possible to implement the model in a hardware description language (HDL), e.g. Verilog-A, and to use it for circuit simulation. To verify the usability of the model for circuit simulation, an inverter consisting of an EGT and a resistor is simulated at 1 V supply voltage (V_{DD}) (Figure 4). The EGT in the pull down network has a *W/L*-ratio of 1 and the resistor in the pull up network has a resistance of 200 kΩ. In Figure 4 the input voltage V_{in} of the inverter is swept from 0 V to 1 V and the output voltage V_{out} is also reaches from 0 V to 1 V.

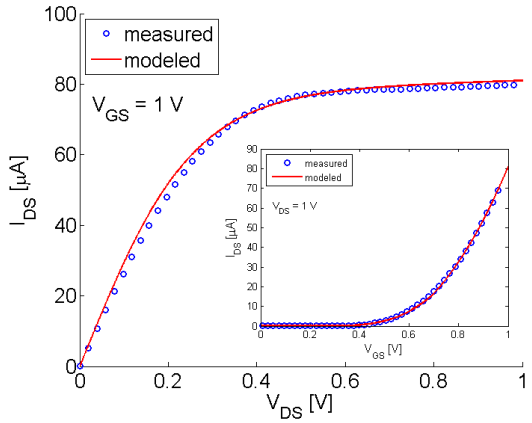

Figure 3: Measured drain-source current versus modeled drain-source current in dependence from the drain-source voltage and the gate-source voltage

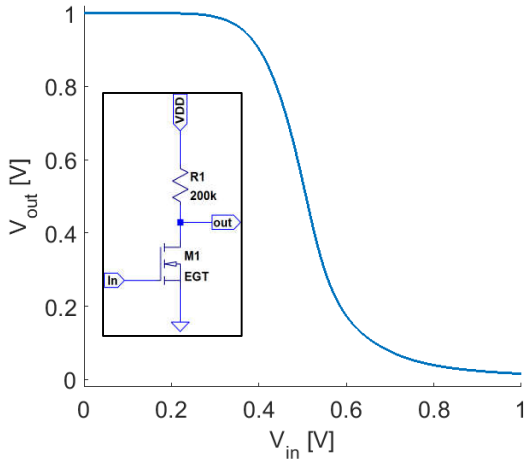

Figure 4: Simulation of an inverter with a resistor in the pull-up network and EGT in the pull-down network

Electrolyte-gated field-effect transistors based on inorganic semiconductor oxides show high DC performance compared with their organic counterparts. In this work, we modeled the DC behavior of such EGTs with different models corresponding to the transistor regimes. The model is implemented with Verilog-A and shows a very good agreement with experimental data. The usefulness of the model for circuit design is shown on the simulation of an inverter.

ACKNOWLEDGEMENT

This work is financially supported by the Helmholtz Gemeinschaft in kind of the Helmholtz Virtual Institute VI530.

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